Modelling and Optimisation of Power Consumption in Reconfigurable Devices

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PhD since Oct. 2009
CAIRN - IRISA

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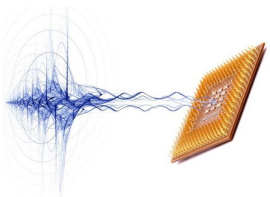
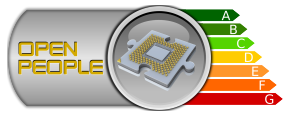
Comité de Suivi de Thèse, CAIRN, 14th February 2010



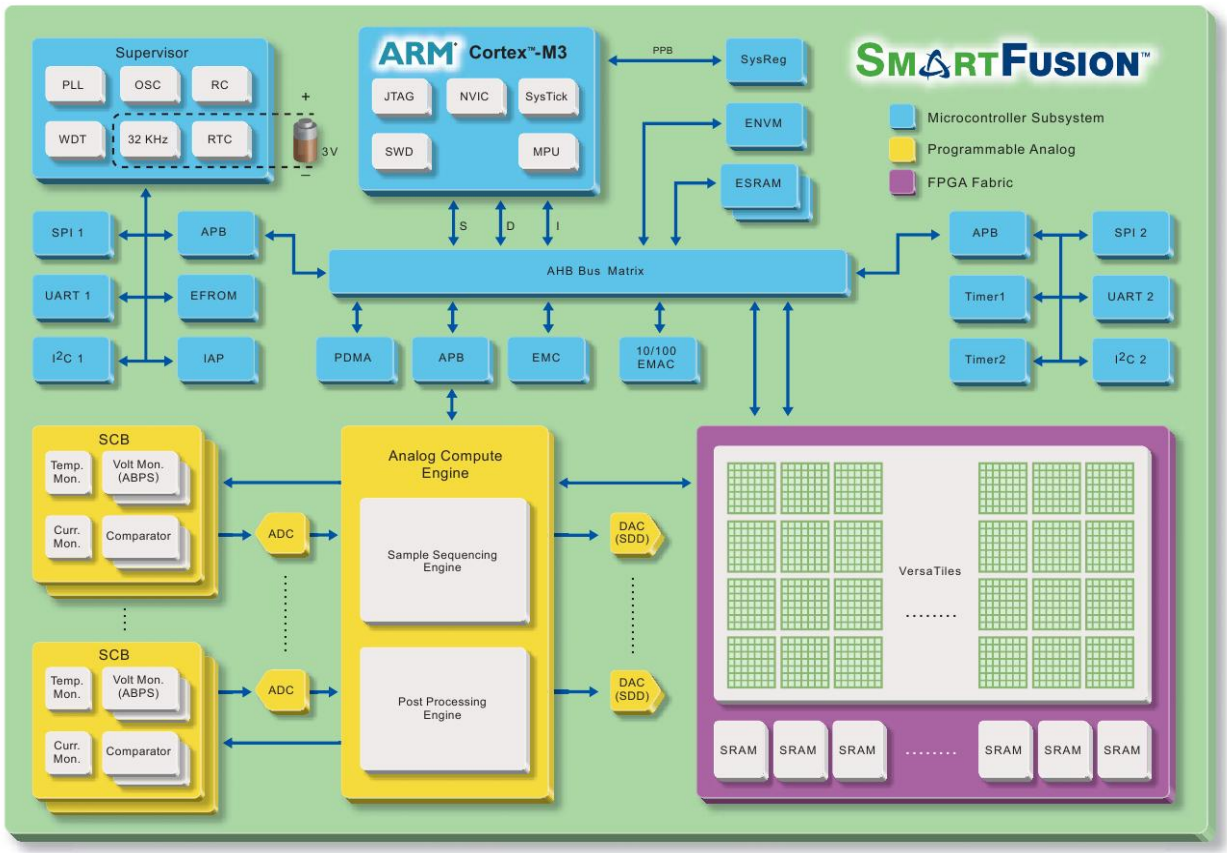
IRISA



System on Chip

SoC : Chip including various functions

- Processor(s)
- Configurable area(s)
- DSP(s)
- Peripheral(s)
- Memory(s)
- Analog



TI : OMAP
Xilinx : Zynq-7000
Actel : SmartFusion

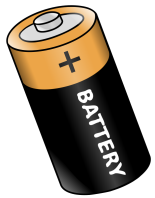
System on Chip

SoC are more and more used

- Size
- Cost

Power consumption

- Battery size/weight
- Dissipation
- Power rails design



Need to have early power estimation for heterogeneous systems

Outline

OpenPEOPLE : Who ?

Consortium :

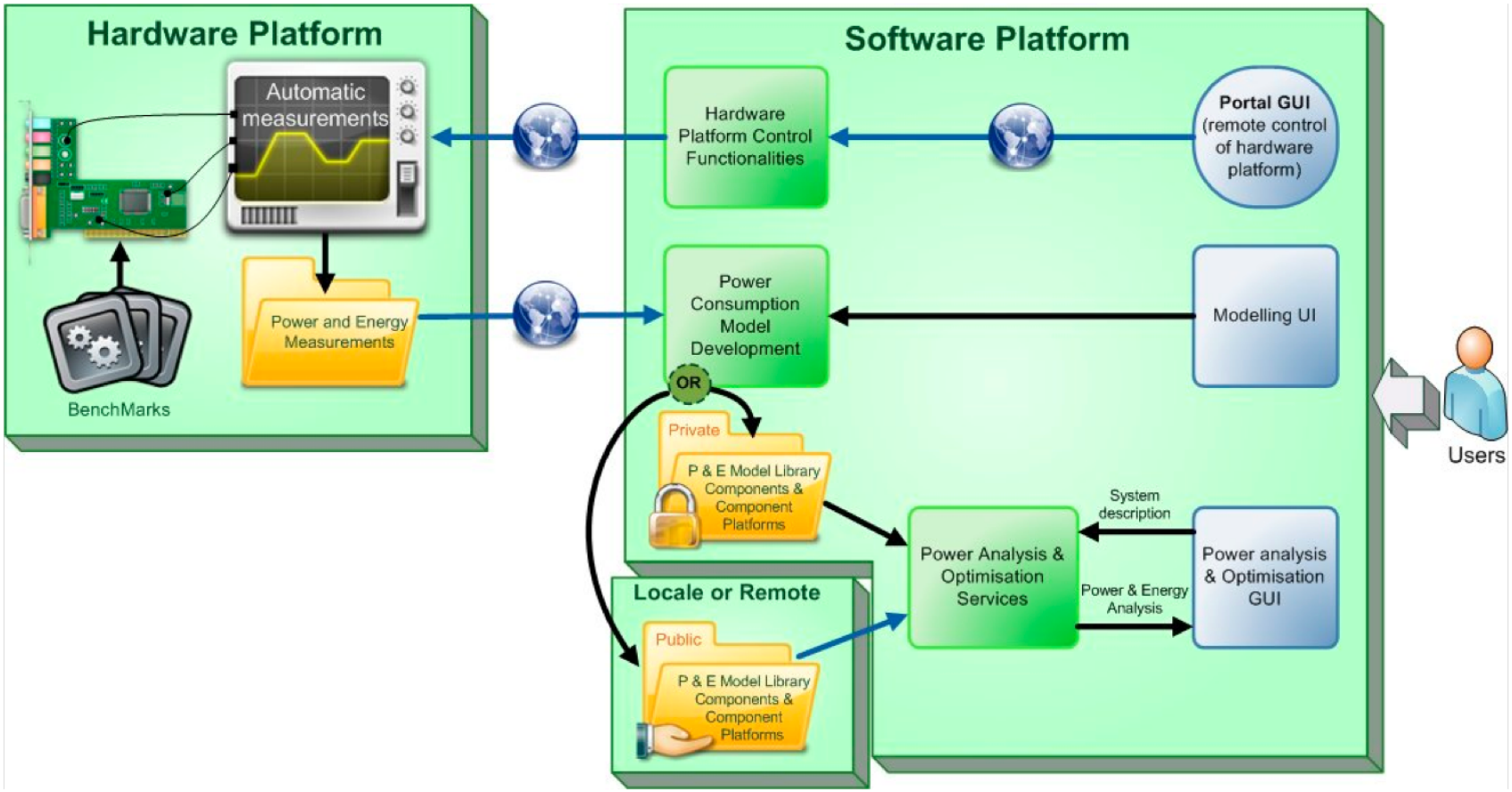
- Lab-STICC - UBS
- LORIA - INRIA Nancy
- Dart - INRIA Lille
- LEAT - UNSA
- IRISA-Cairn - UR1
- THALES Coms. - Colombes
- InPixal - Rennes

Project funded by the ANR

OpenPEOPLE : What is it ?

Open-PEOPLE :

Open-Power and **E**nergy **O**ptimization **PL**atform and **E**stimator



OpenPEOPLE : What for ?

Complete platform to

- allow rapid power and energy estimation and measurement for complex heterogeneous systems
- test the effects of different optimizations on power consumption

CAIRN : Power consumption models for hardware tasks and reconfiguration

- Rachid DRIF (2009)
- Abdoulaye SARRE (2009-2010)
- Ferhat ABBAS (2010)
- Rim ABID (2011)

Outline

CMOS Power Consumption [Julien06], [Garcia99], [TI97]

- Dynamic Power
  - Voltage ^{2}
  - Frequency
  - Activity
  - Load (Nets Capacitance)

$$P_d = {V_{cc}}^2 \times F \times \alpha \times C$$

CMOS Power Consumption [Julien06], [Garcia99], [TI97]

- Dynamic Power
  - Voltage ^{2}
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  - Activity
  - Load (Nets Capacitance)

$$P_d = {V_{cc}}^2 \times F \times \alpha \times C$$

- Static Power (Leakage)
  - Area, Occupation Rate
  - Voltage

$$P_s = V_{cc} \times A$$

Power Modelling

- Fine Grain
  - Activity
  - Net length
  - Flip-flops
  - Operators
- Coarse Grain
  - Application parameters
  - RAM
  - Area
  - Delay

Pb : Power estimation done late

Pb : Bad power estimation accuracy

Power Modelling

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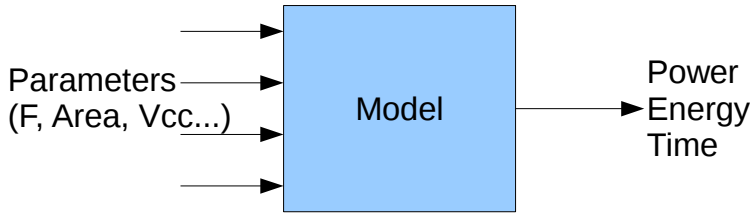
Pb : Bad power estimation accuracy

- State Machine models [Benini00]
- Peak consumption [Gupta03]
- Glitches [Ragh96]
- ...

Model ?

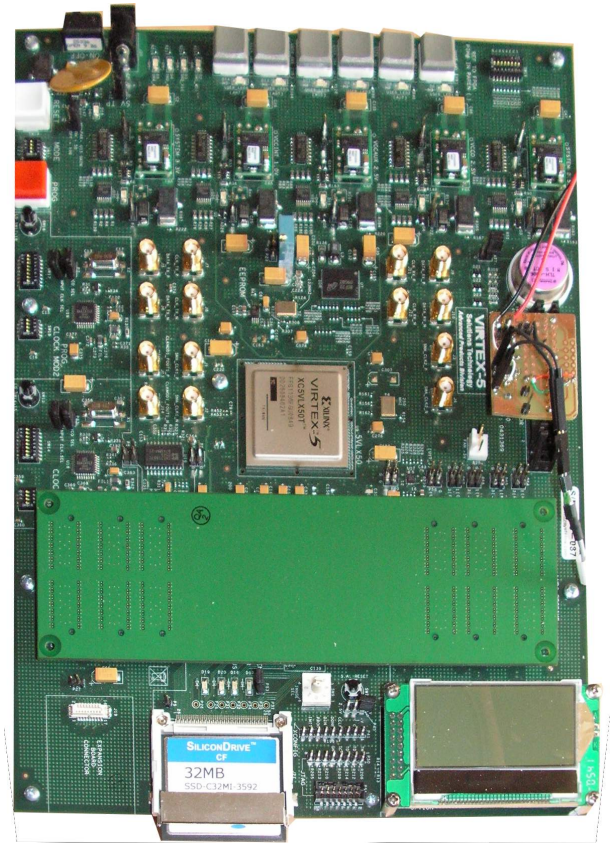


- What is a model ?
  - P/E = f(parameters)

- How to build a model ?
  - Measurements following parameters
  - Analysis, Statistics
  - Verification

Xilinx ML550 Board

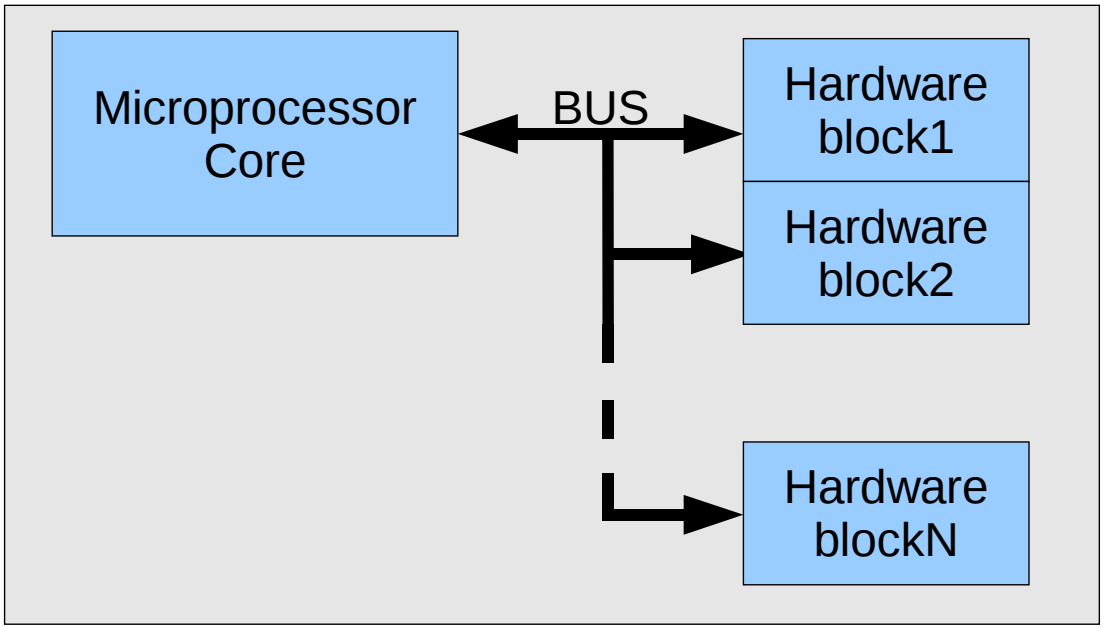
- FPGA Virtex-5 VLX50T (7200 slices)
- SystemACE CompactFlash controller
- 5 power rails (core, IOs, peripherals)
- Current sense resistors



Previous work on Actel IGLOO.
Future work planned on Virtex 6, Altera Stratix.

Outline

Hardware Blocks

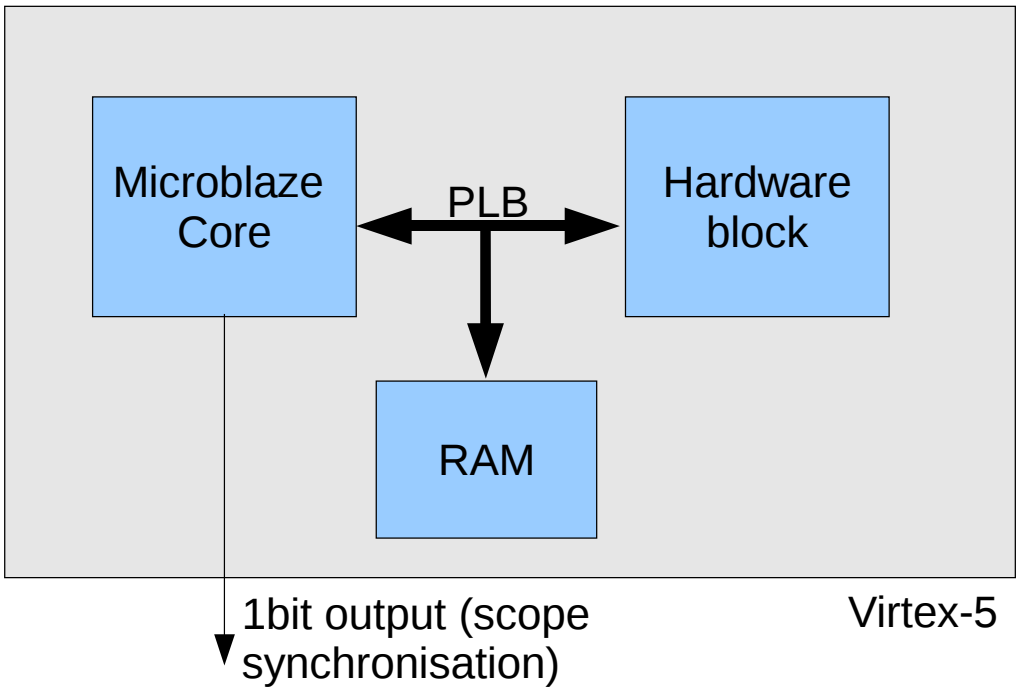


- unload processor core
- Power/Energy/Throughput efficiency [AlteraAN531]
- parallelism level

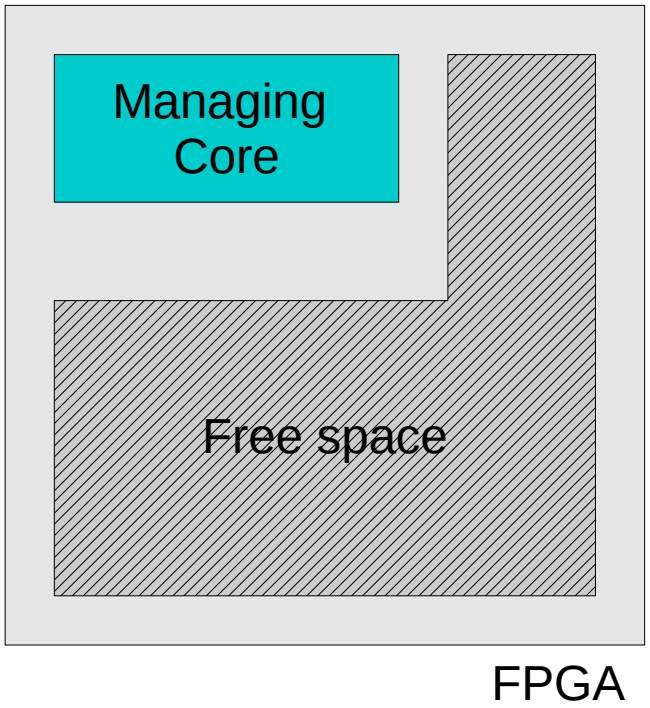
C to VHDL

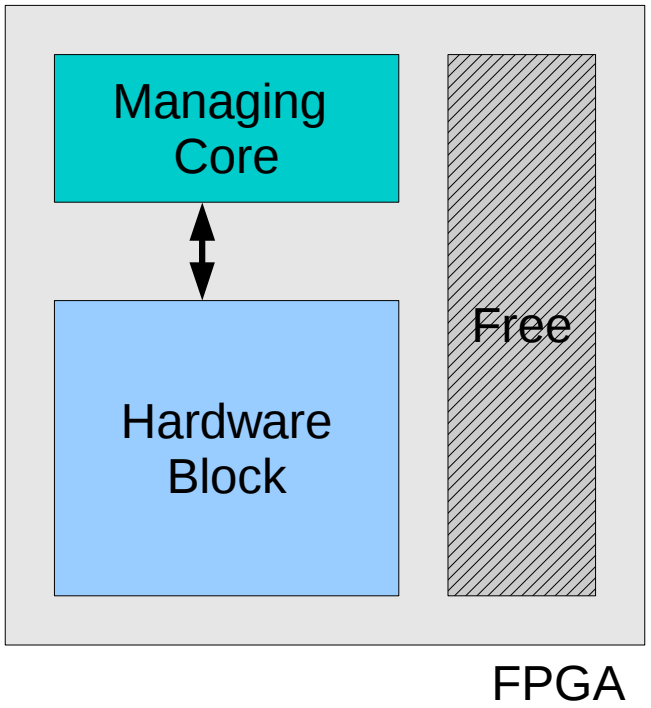
Effect of parallelism level on Power consumption

- Generation of hardware blocks
- High level synthesis (C to VHDL)
- Loop unrolling
- PLB block, Microblaze at 100MHz



Measurement Protocol





- Idle power consumption
- Active power consumption
- Execution Time

Matrix Multiplication C code

```
for (i = 0; i < M; i++)
    for (j = 0; j < P; j++)
        _C[i][j] = 0;

for (i = 0; i < M; i++)                    //(loop 1)
    for (k = 0; k < N; k++)                //(loop 2)
        for (j = 0; j < P; j++)            //(loop 3)
            _C[i][j] += _A[i][k]*_B[k][j];
```

Loop Unrolling Index (LUI) notation :
LUI_1, LUI_2, LUI_3

Ex of Power Consumption Measurement

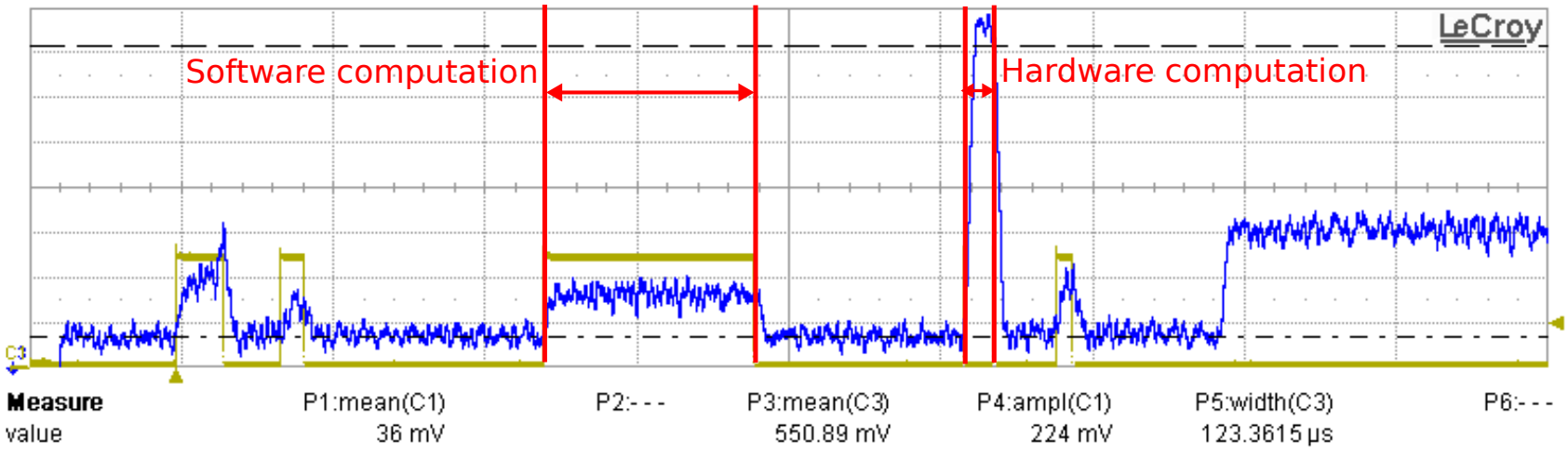


Figure 1: Power consumption measurements : matrix multiplication software and hardware executed (blue).

Execution time versus Loop Unrolling Index

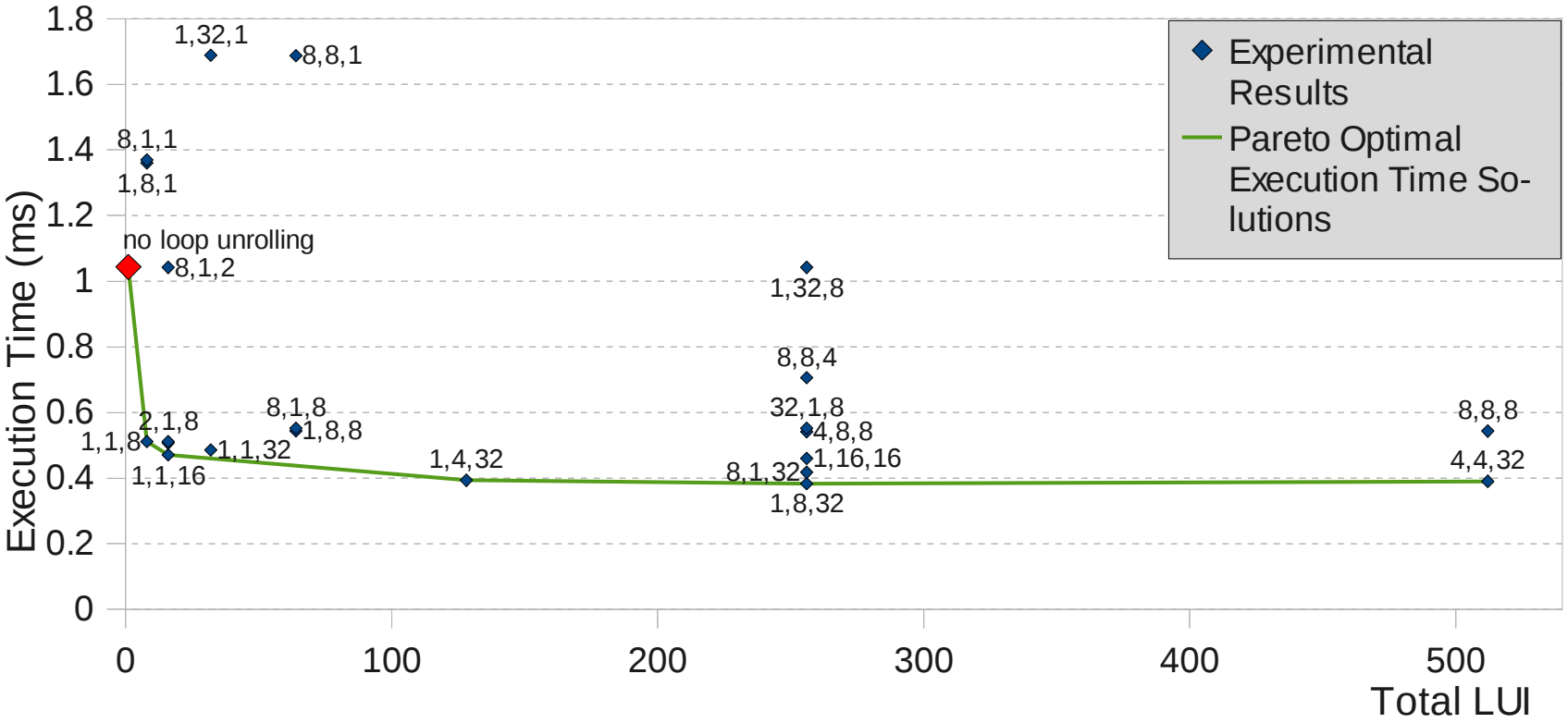


Figure 2: Power consumption measurements : matrix multiplication execution time versus total loop unrolling index.($LUI1, LUI2, LUI3$)

Energy consumption versus Loop Unrolling Index

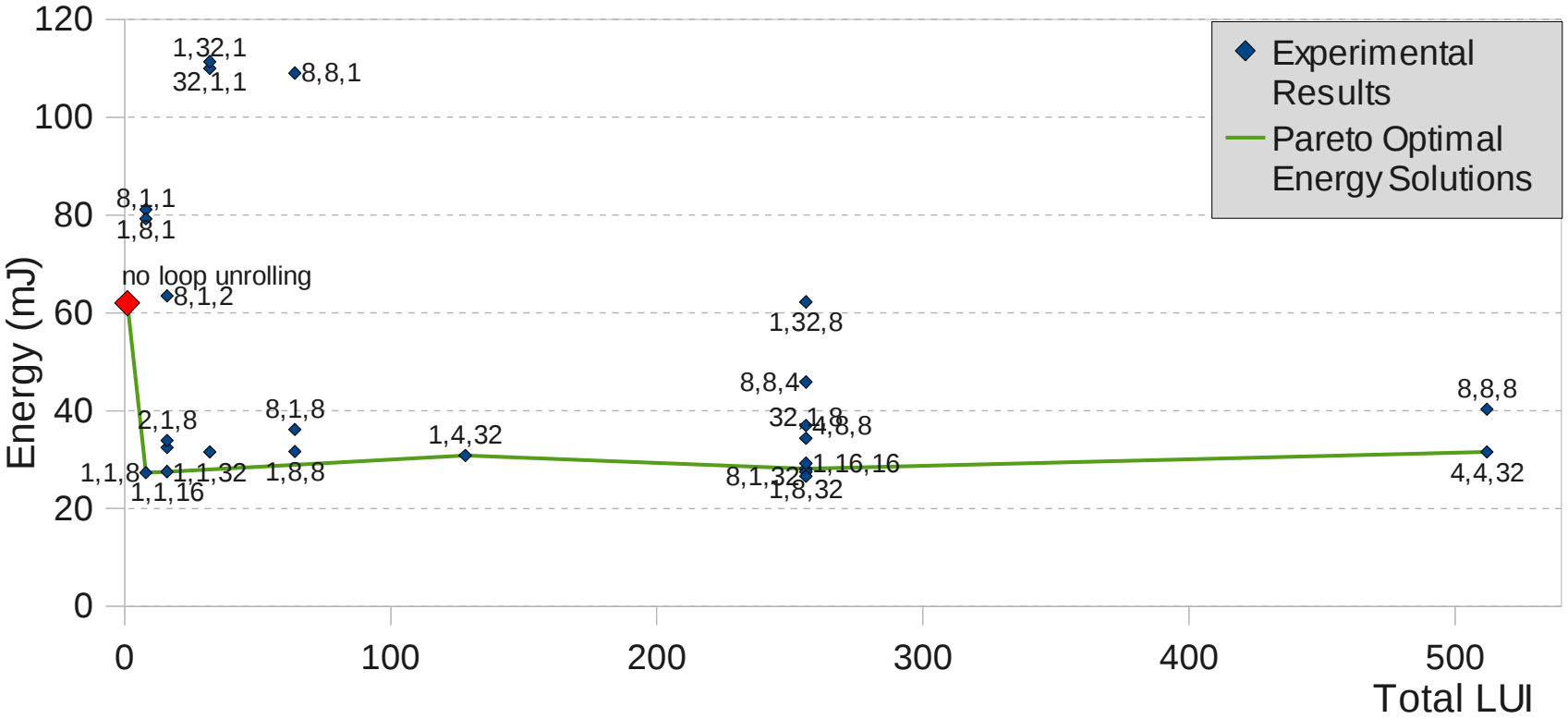


Figure 3: Power consumption measurements : matrix multiplication energy consumption versus total loop unrolling index.($LUI1, LUI2, LUI3$)

Energy vs. Execution Time

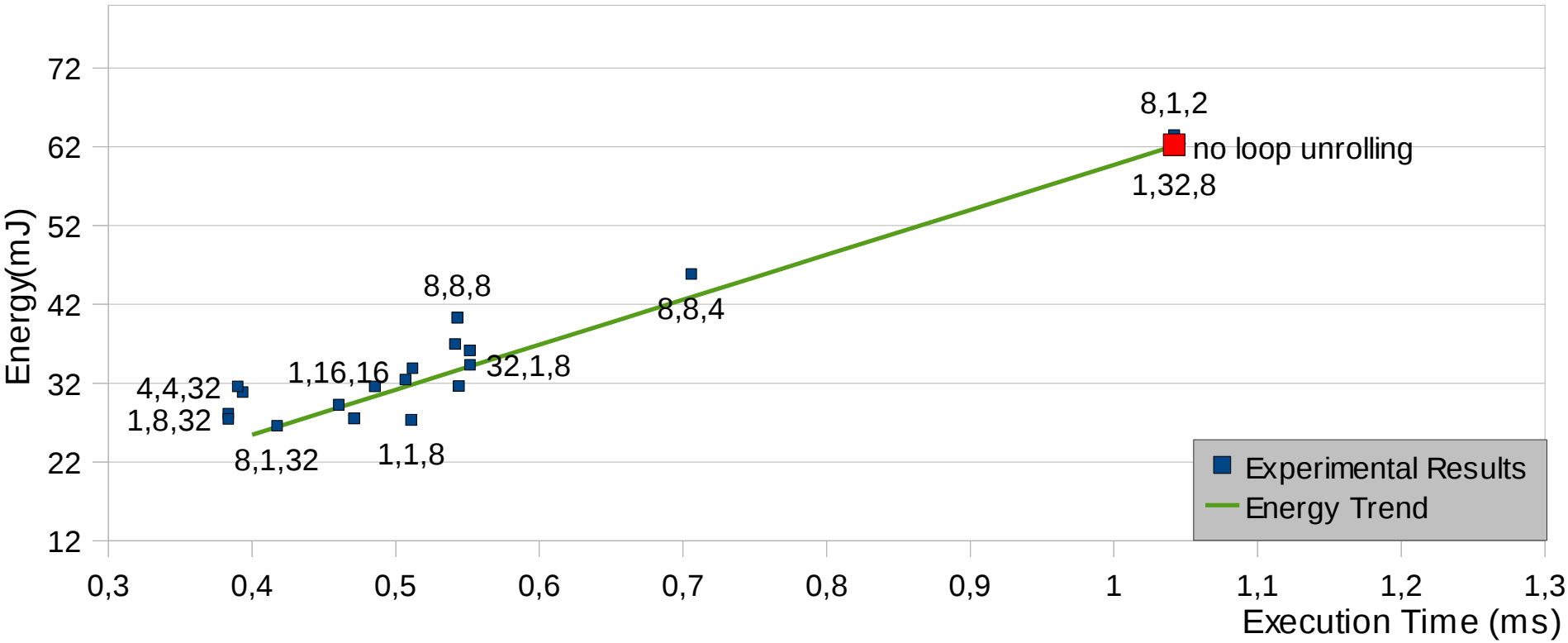


Figure 4: Energy of the matrix multiplication versus execution time.($LUI1, LUI2, LUI3$). Trend $E = A + B \times t$.

Power and Parallelization

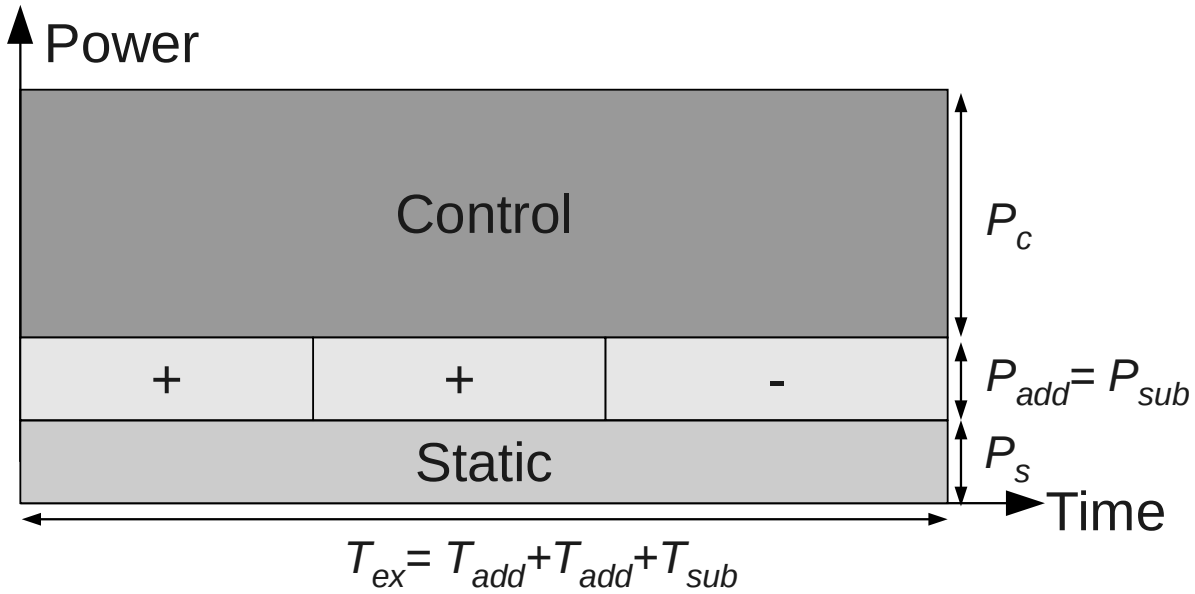
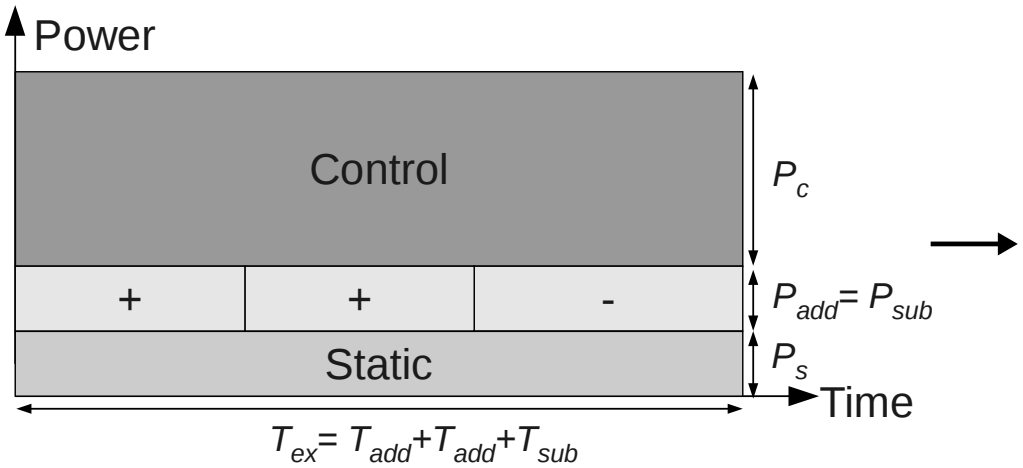


Figure 5: Representation of power consumption for a hardware task

Power and Parallelization



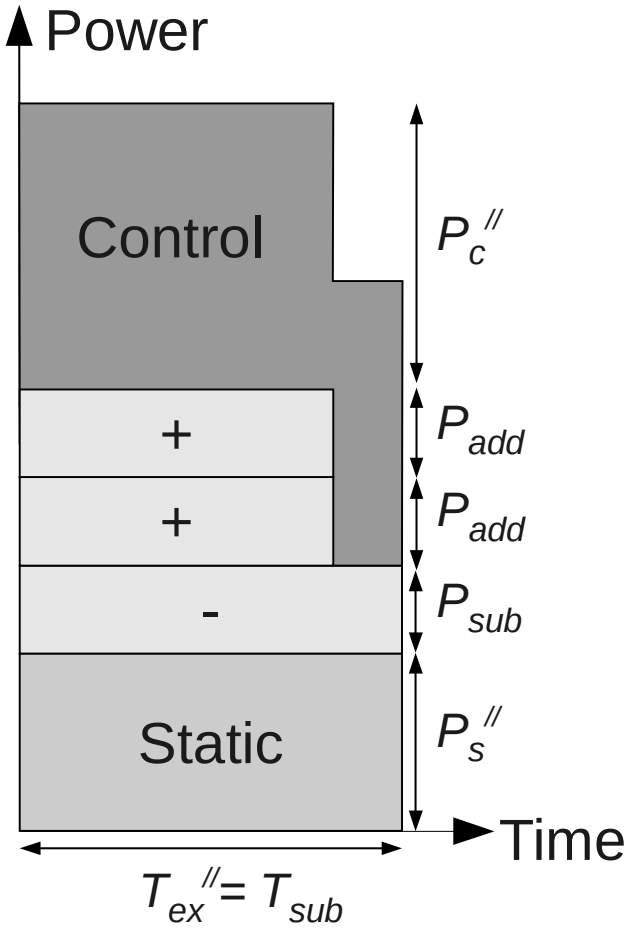


Figure 5: Representation of power consumption for a parallelized hardware task

- Experiments on two more complex algorithms used in video :
  - part of Full Search
  - Deblocking Filter
- Energy is not a constant

$\rightarrow$ When space is available, exploit parallelism of each task

- Experiments on two more complex algorithms used in video :
  - part of Full Search
  - Deblocking Filter
- Energy is not a constant

→ When space is available, exploit parallelism of each task

↗ parallelism level
↗ area
↗ bitstream
→ Impact of reconfiguration ?

Outline

Dynamic Partial Reconfiguration

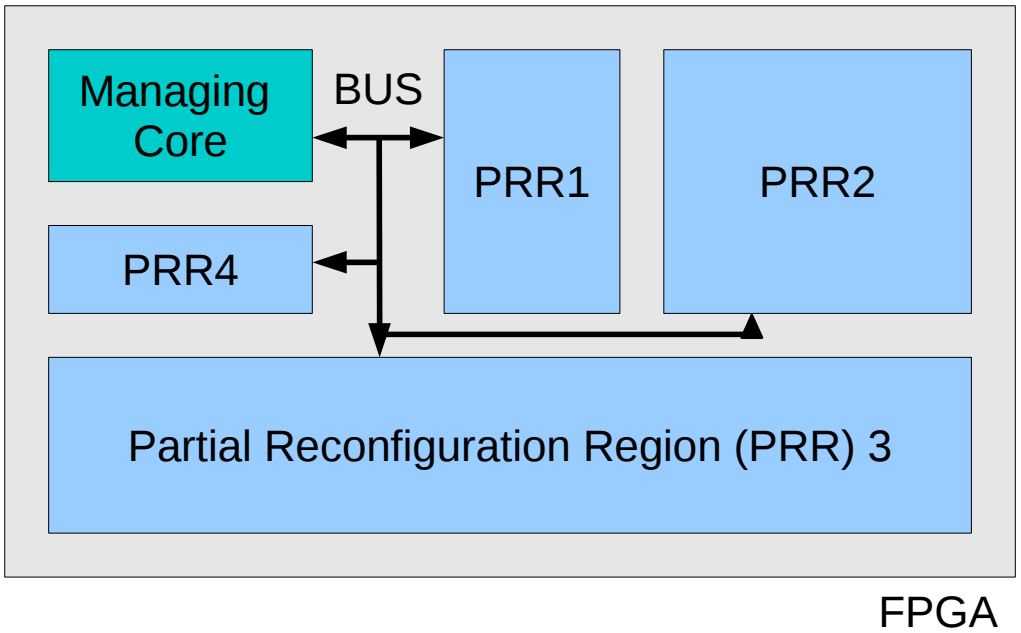
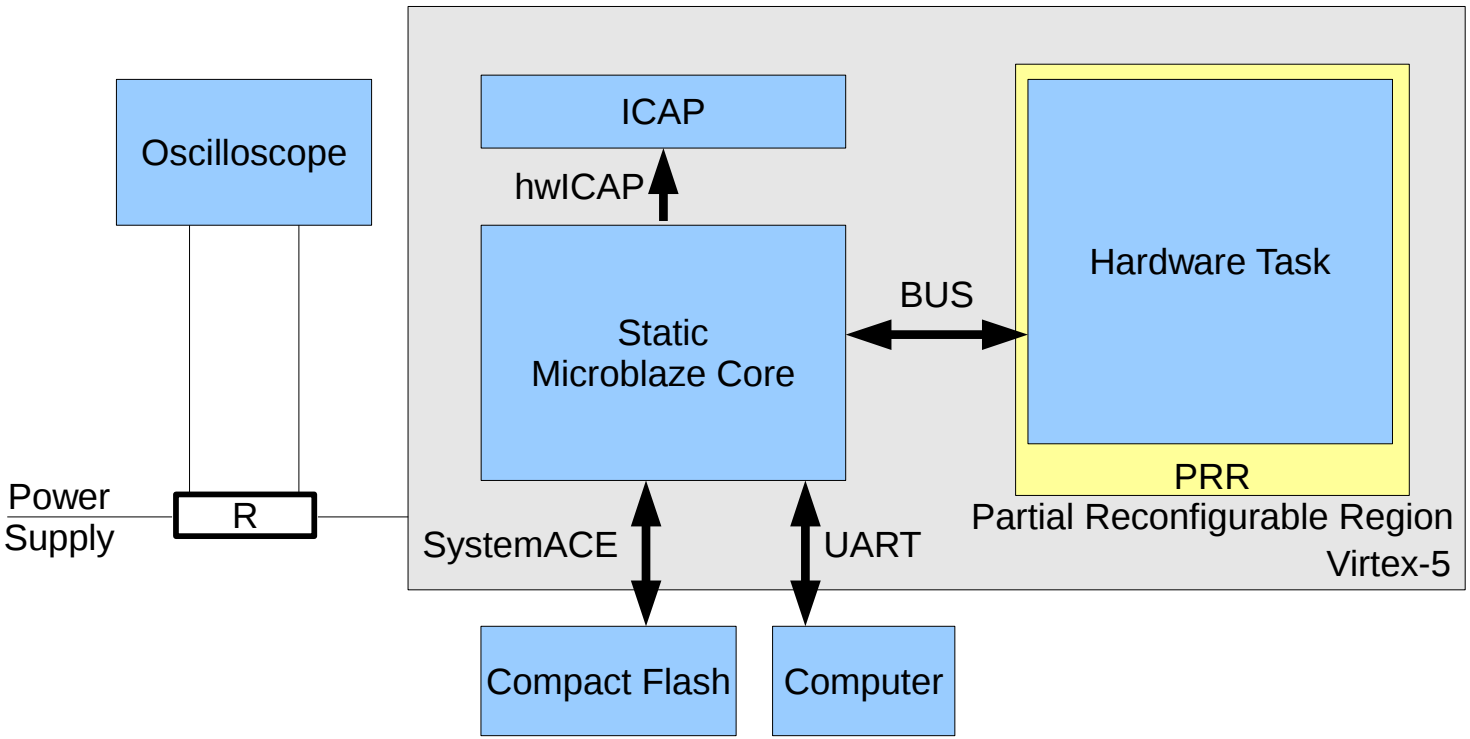


Figure : Partial Reconfiguration segmentation example

Partial reconfiguration (PR) is studied for space and energy saving. [Savary07], [Becker03]
No detailed model for PR power consumption

Dynamic Partial Reconfiguration

A Microblaze soft. core and a hardware task.

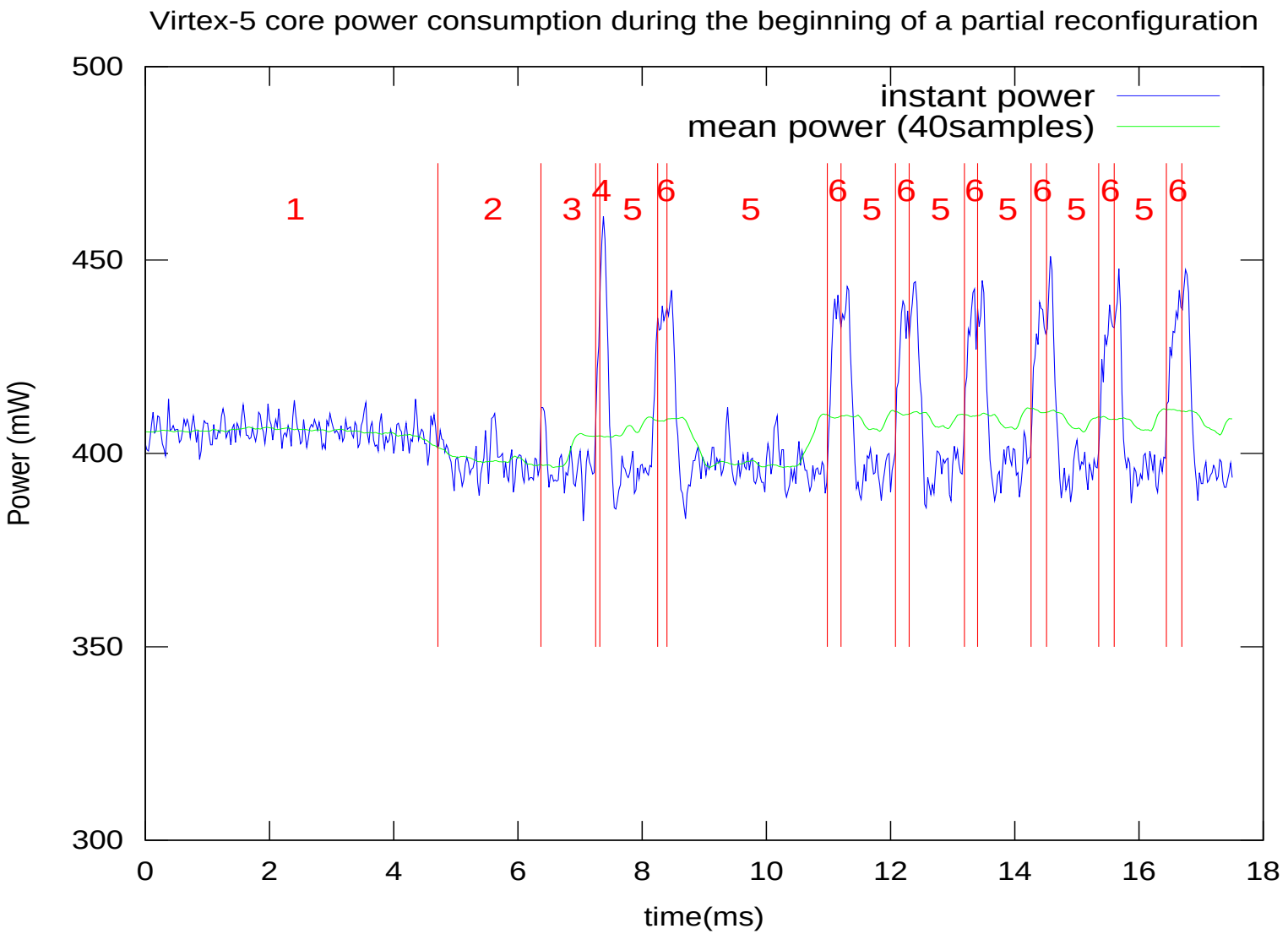


PR Steps

(1) reconfiguration **order** arrives
(2) **open** bitstream's file
(3) **read** bitstream's header
(4) **check** header's validity
(5) **read** of a bitstream sector
(6) **write** data to ICAP (Internal Configuration Access Port)
(7) repeat (5) and (6) until the end of the bitstream.

Power Consumption at the Beginning of PR

(2) **open**
(3) **read**
(4) **check**
(5) **read**
(6) **write**



Power Consumption during PR

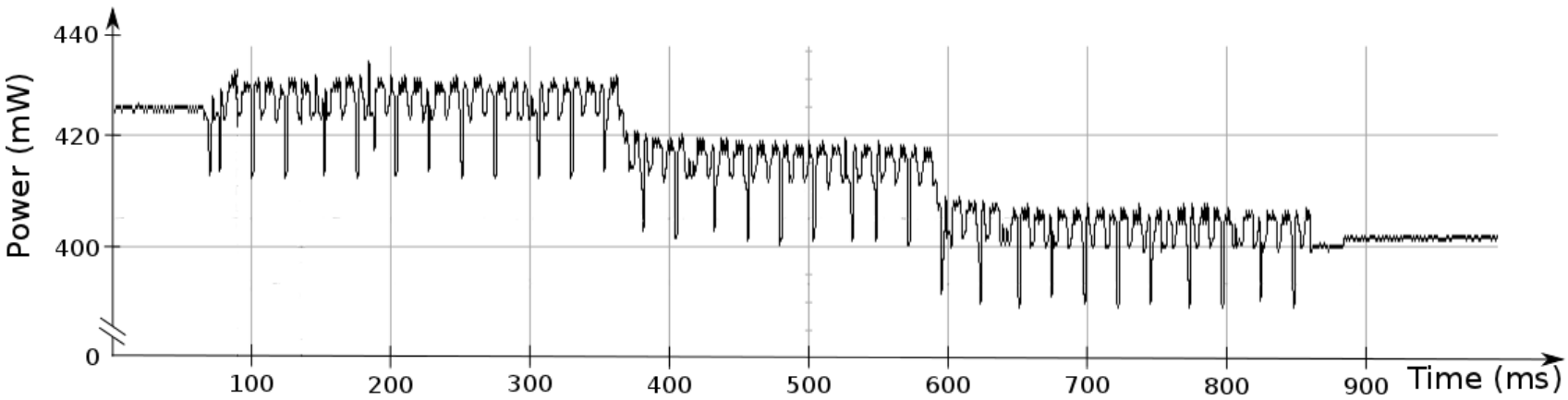


Figure : Partial Reconfiguration of PRR from a matrix multiplication hardware task to a low power task

Parameters

Parameters that affect energy consumption

- Memory access
- Activity of the managing core (Read and write)
- PRR Area/Bitstream size
- Difference with the previous configuration

Parameters that don't affect energy consumption

- Shape of the Partial Reconfiguration Region
- Bitstream composition

Parameters to study

- Other memory, soft processor, ICAP IP, device

Trivial model (Virtex5 VLX50T) :

$E \simeq 39\mu J$ *per* kB with CF, microblaze @ 100MHz, Vcore=1V

Conclusion

Power consumption of tasks :

- Increasing the parallelism level increases the area but reduces energy consumption
- Set of measures for different versions of an algorithm : Power, Execution Time, Energy, Area

Power consumption of the reconfiguration :

- Lot of parameters to extract
- Energy consumption is highly related to the region size

Future Work

Power consumption of tasks :

- High level tool to "measure" parallelism level of tasks

Comparison with other devices (Virtex 6)

Goal

Library of tasks and reconfiguration models

- Estimation and Optimization for Open-PEOPLE platform
- Power manager to reconfigure tasks on-the-fly

CST information

- Problems
  - Power measurements with resistors
  - Board support
  - Time for measures, reconfiguration projects
- Training
  - ECOFAC (19.5h)
  - IEEE Distinguished Lectures (2h)
  - No professional and general courses
- Publications
  - ARC 2011 (rejected)
  - NEWCAS 2011 (rejected)
  - HEART 2011 (submitted)
  - ReCoSoc 2011 (submitted)
- Presentations
  - Each Open-PEOPLE project meeting
  - CAIRN Team seminar
- 2 month per year at LEAT

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