Power Consumption Modeling of Reconfigurable Architectures and Dynamic Reconfiguration

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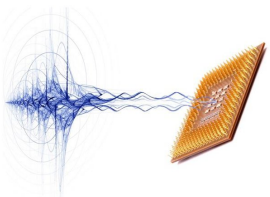
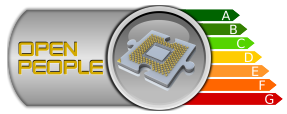


IRISA



Outline

OpenPEOPLE : Who ?

Consortium :

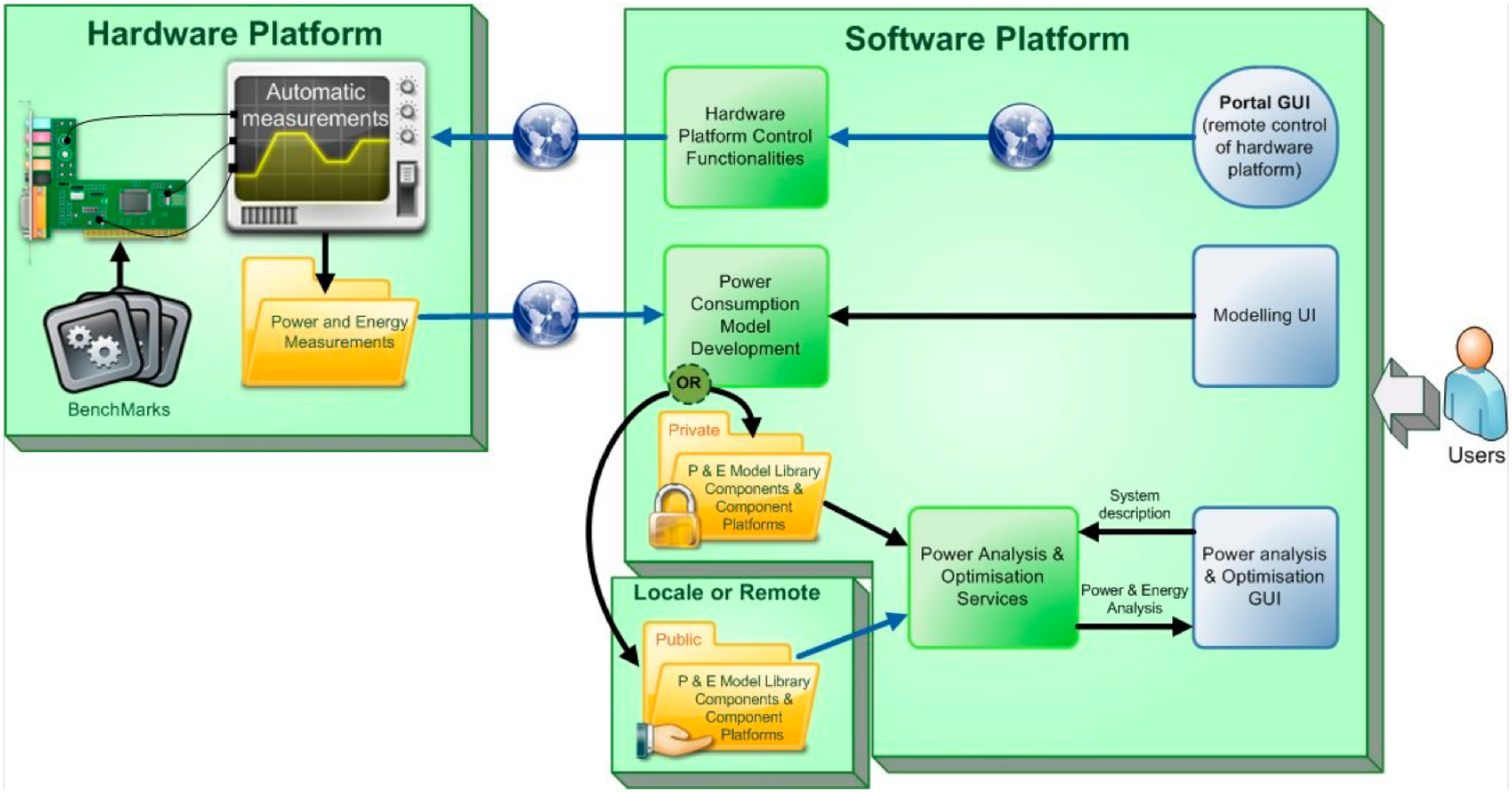
- Lab-STICC - UBS
- LORIA - INRIA Nancy
- Dart - INRIA Lille
- LEAT - UNSA
- IRISA-Cairn - UR1
- THALES Coms. - Colombes
- InPixal - Rennes

Project funded by the ANR

OpenPEOPLE : What is it ?

Open-PEOPLE :

Open-Power and **E**nergy **O**ptimization **PL**atform and **E**stimator



OpenPEOPLE : What for ?

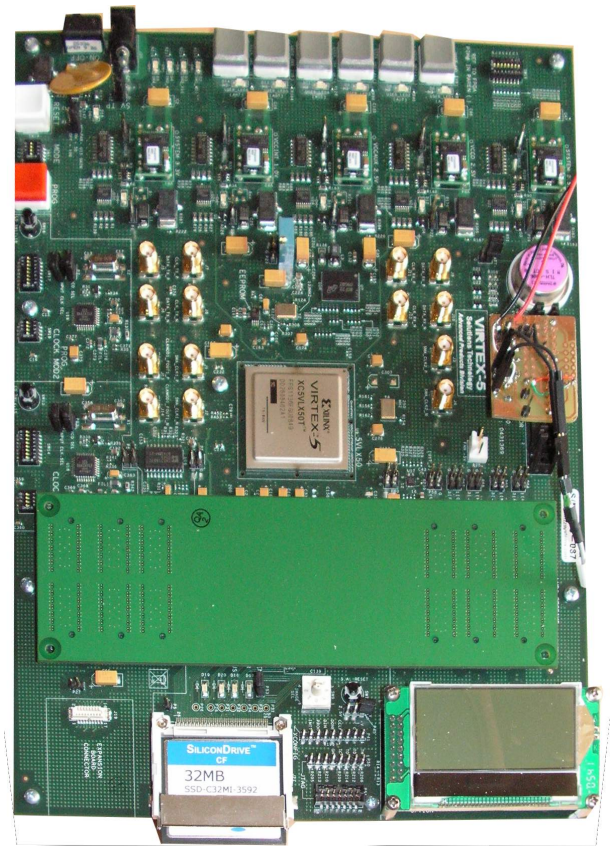
Complete platform to

- allow rapid power and energy estimation for complex heterogeneous systems
- test the effects of different optimizations on power consumption

CAIRN : Power consumption models for hardware tasks and reconfiguration

Xilinx ML550 Board

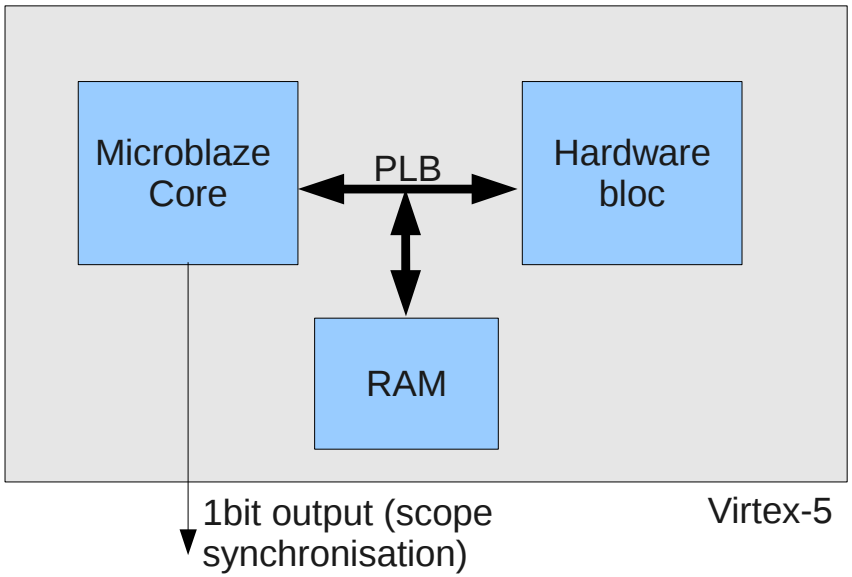
- FPGA Virtex-5 VLX50T (7200 slices)
- SystemACE CompactFlash controller
- 5 power rails (core, IOs, peripherals)
- Current sense resistors



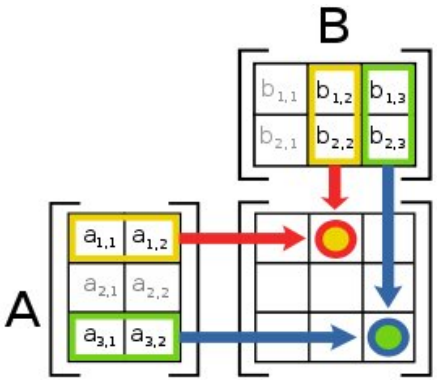
C to VHDL

- Generation of hardware blocks
- High level synthesis
- PLB block
- Microblaze @ 100MHz
- DMA

Effect of loop unrolling



Matrix multiplication



$$(A \times B)_{i,j} = \sum_{k=1}^{n} A_{i,k} \times B_{k,j} \quad (1)$$

- $32 \times 32 \times 32$, $8bit$
- 3 nested loops (32768 *op*)
- static loops

C code

```
for (i = 0; i < M; i++)
    for (j = 0; j < P; j++)
        _C[i][j] = 0;

for (i = 0; i < M; i++)                    //(loop 1)
    for (k = 0; k < N; k++)                //(loop 2)
        for (j = 0; j < P; j++)            //(loop 3)
            _C[i][j] += _A[i][k]*_B[k][j];
```

Ex of Power Consumption Measurement

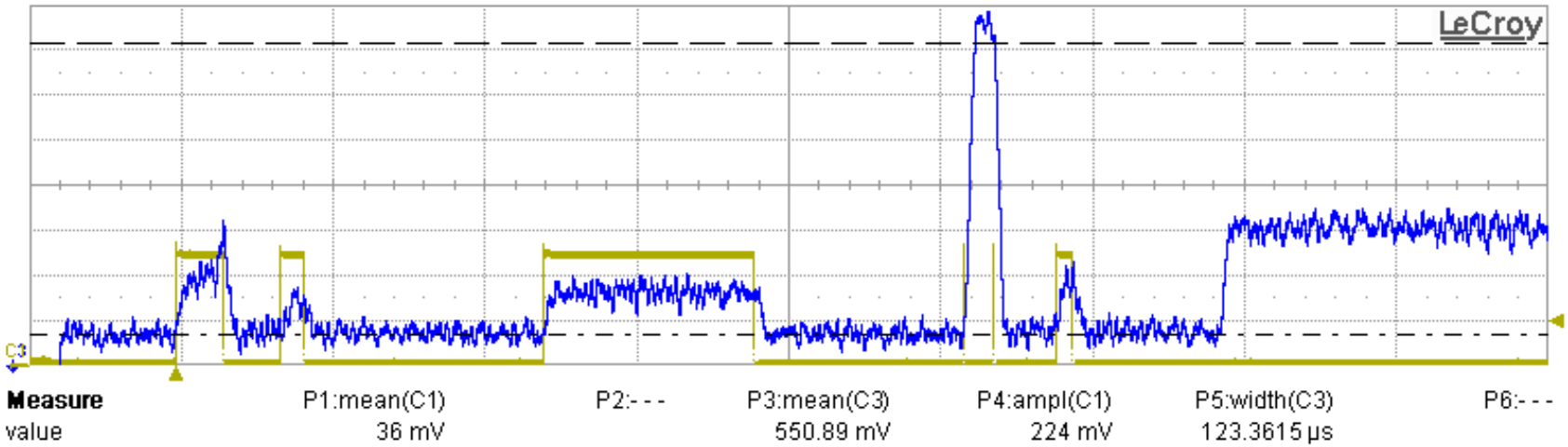


Figure 1: Power consumption measurements : matrix multiplication software and hardware executed (blue).

Energy vs. Execution Time

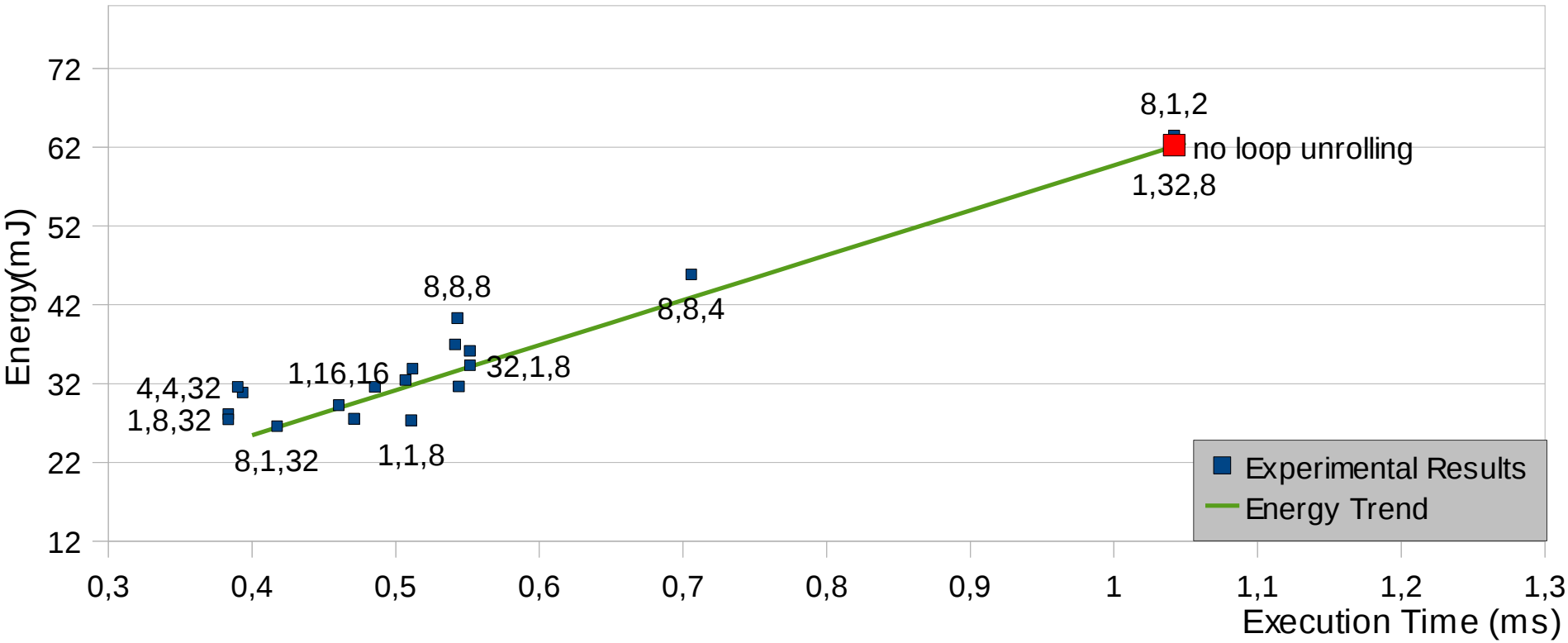


Figure 2: Energy of the matrix multiplication the execution time. Trend equation is $E\{mJ\} = 2.64\{mJ\} + 0.057\{W\} \times t\{ms\}$.

Power and Parallelization

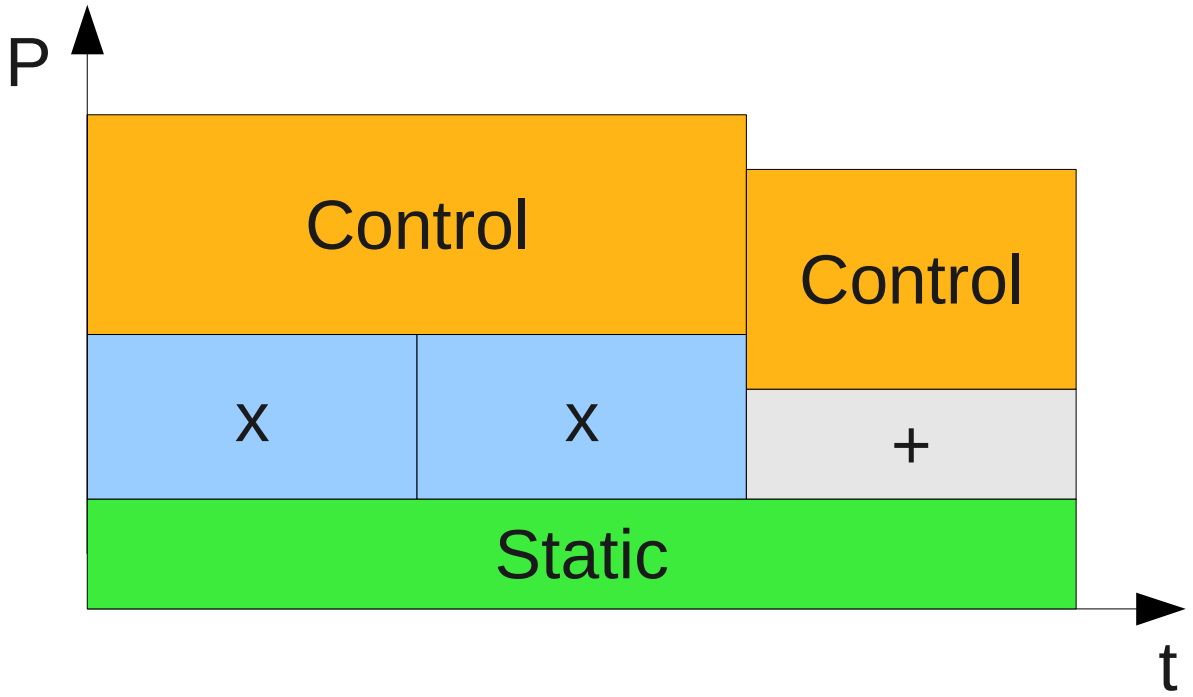
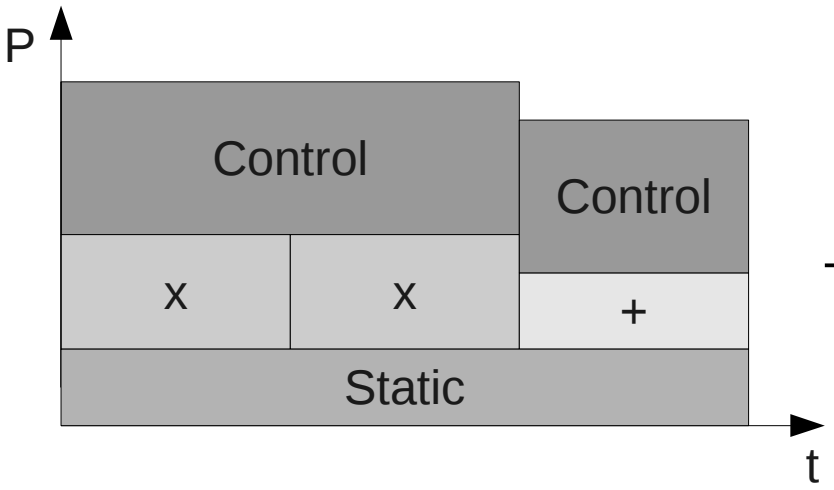
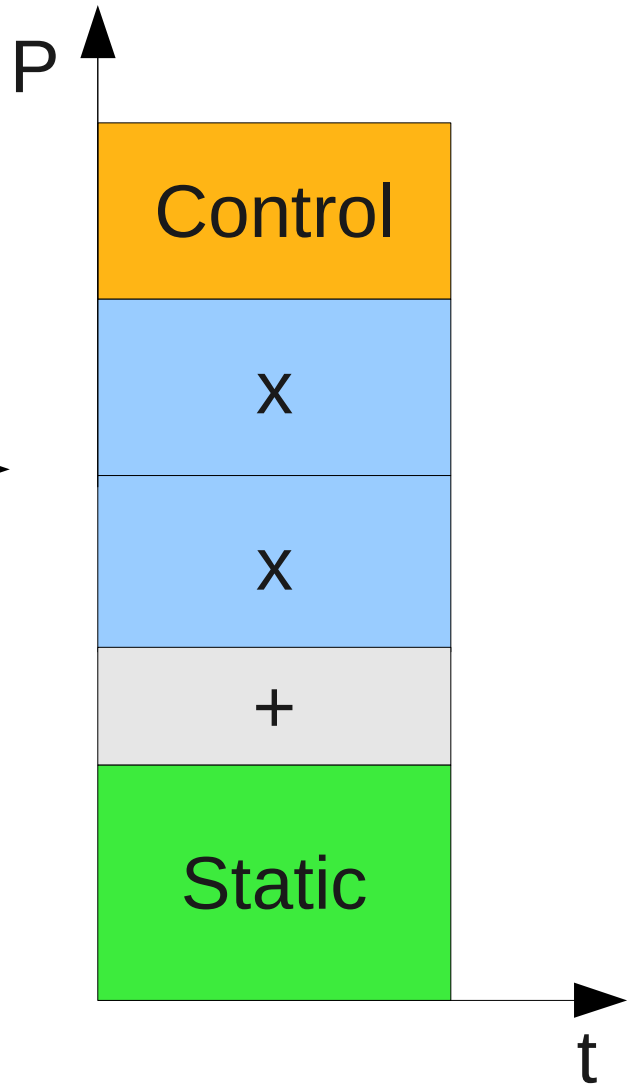


Figure 3: Representation of power consumption for a hardware task

Power and Parallelization





- Experiments on two additional algorithms
- Energy is not a constant

$\rightarrow$ Exploit parallelism of each task

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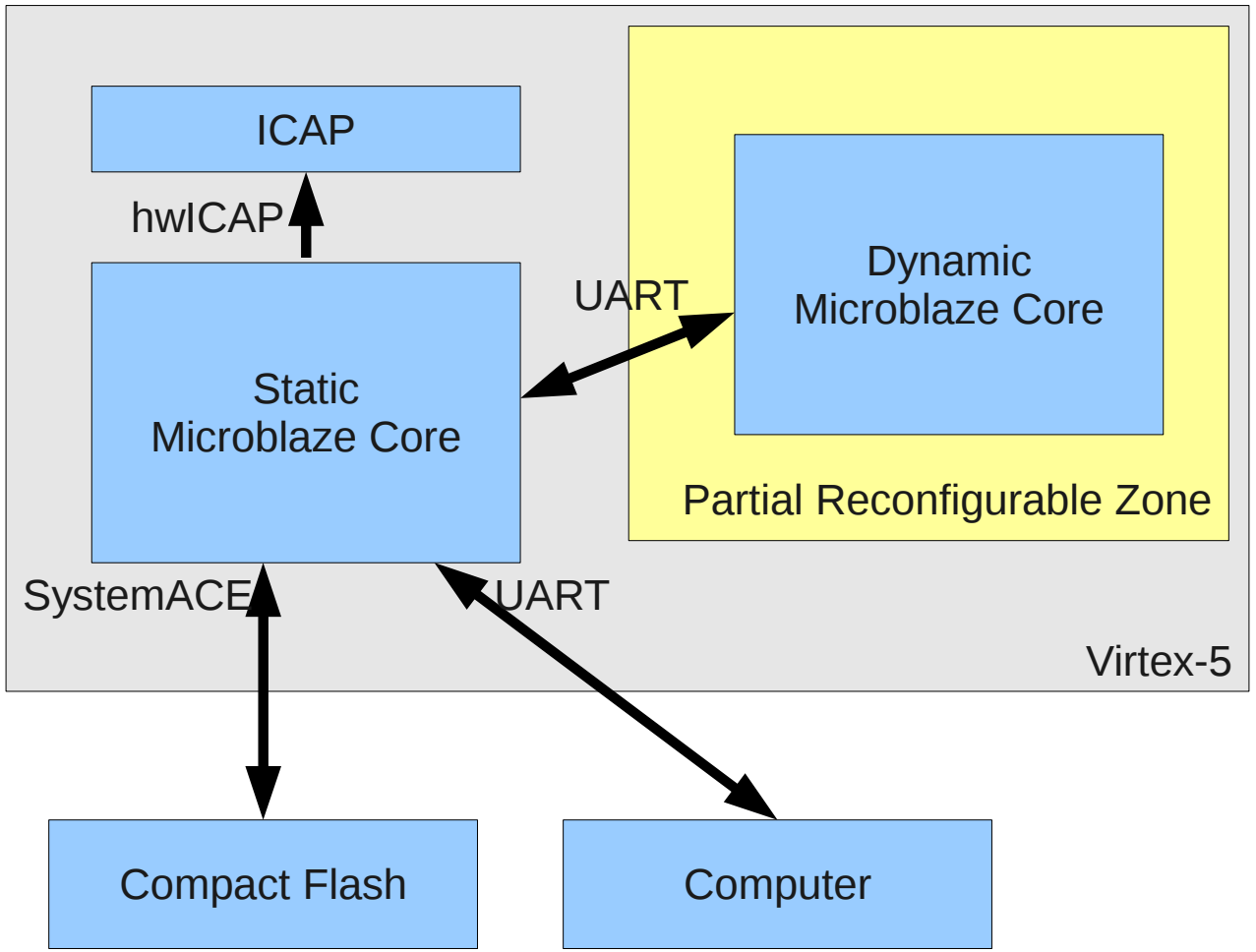
Impact of reconfiguration ?

Outline

Dynamic Partial Reconfiguration

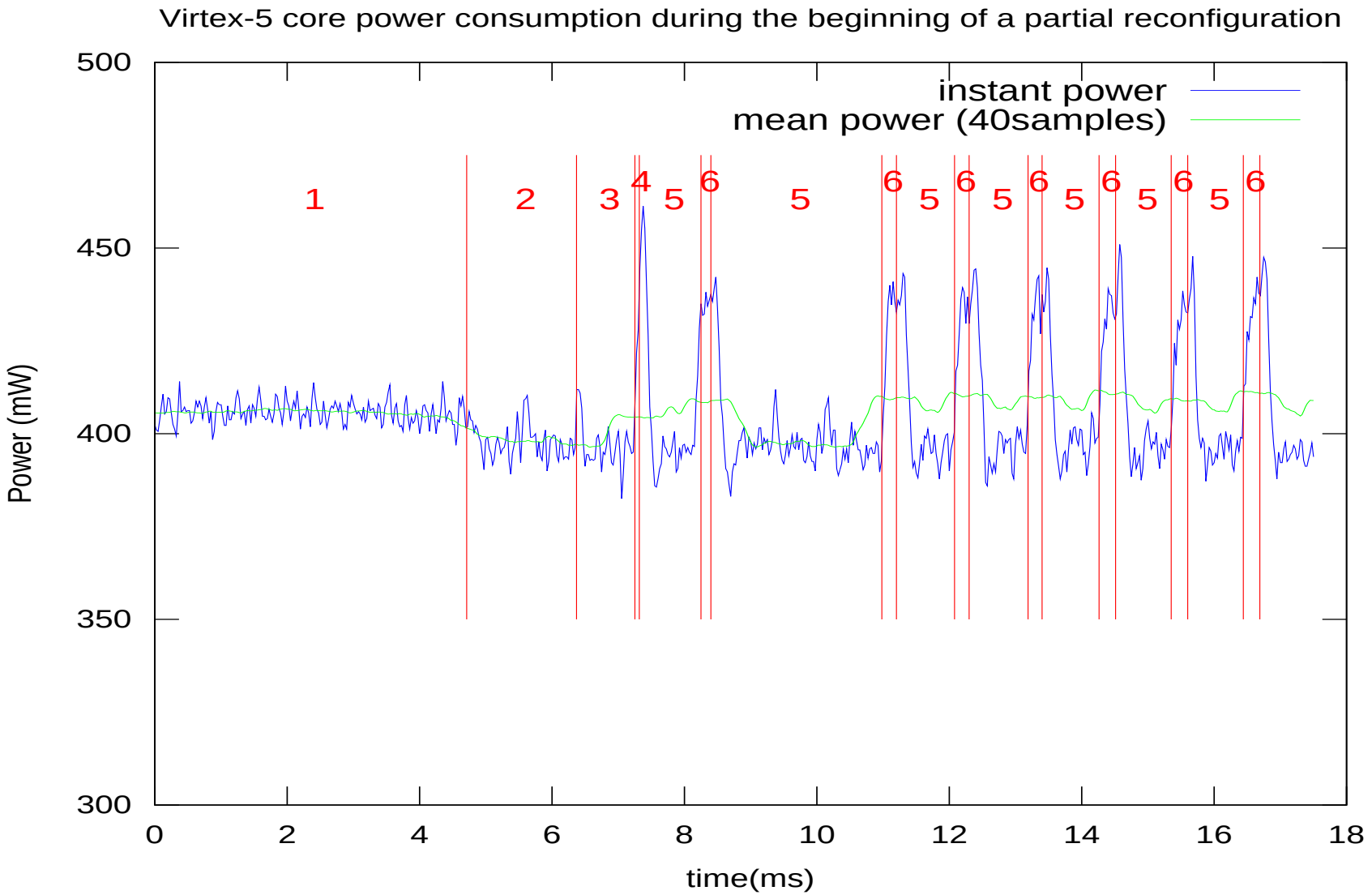
Two Microblaze soft. cores.
One static manages the reconfiguration of the second.



PR Steps

(1) reconfiguration **order** arrives
(2) **open** bitstream's file
(3) **read** bitstream's header
(4) **check** header's validity
(5) **read** of a bitstream sector
(6) **write** data to ICAP (Internal Configuration Access Port)
(7) repeat (5) and (6) until the end of the bitstream.

Power Consumption at the Beginning of PR



Parameters

Parameters that affect energy consumption

- Activity of the managing core (File System...)
- Bitstream size

Parameters that don't affect energy consumption

- Shape of the Partial Reconfiguration Region
- Difference with the previous configuration

Parameters to study

- Bitstream composition

Trivial model (Virtex5 VLX50T) :

$E \simeq 39\mu J \ per \ kB$

Conclusion

- Energy decreases with loop unrolling
- First model
- PR impacts energy and delay
- First trivial model

Future Work

- High-level parser
- Measurements for different reconfigurable blocks
- Scheduler to optimize the energy